Fig.1 (Prior Art)

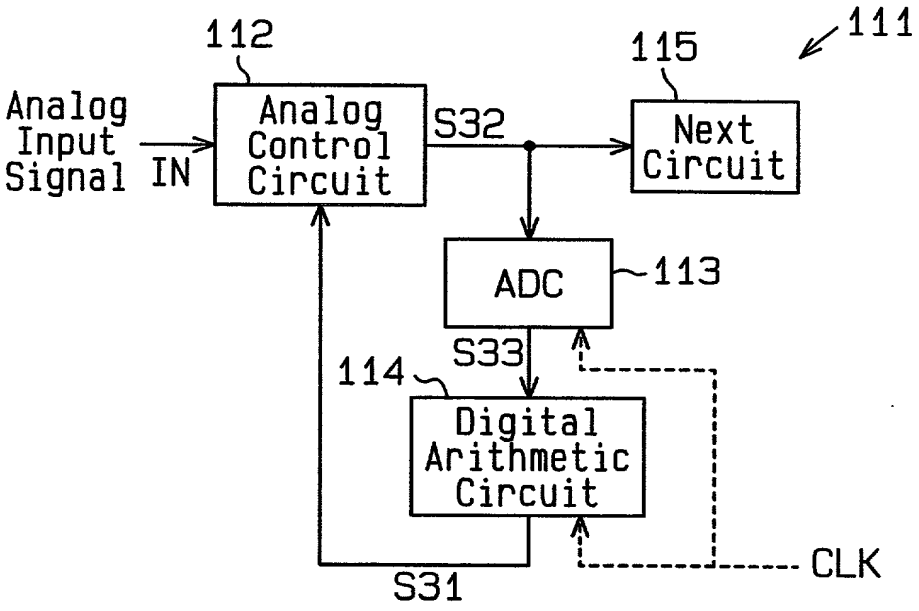


Fig.2 (Prior Art)

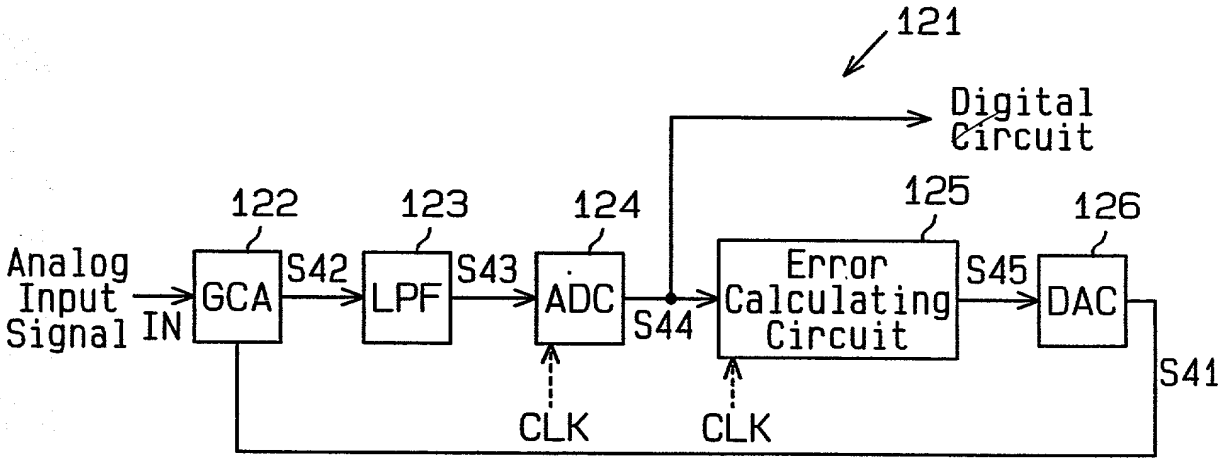


Fig.3(Prior Art)

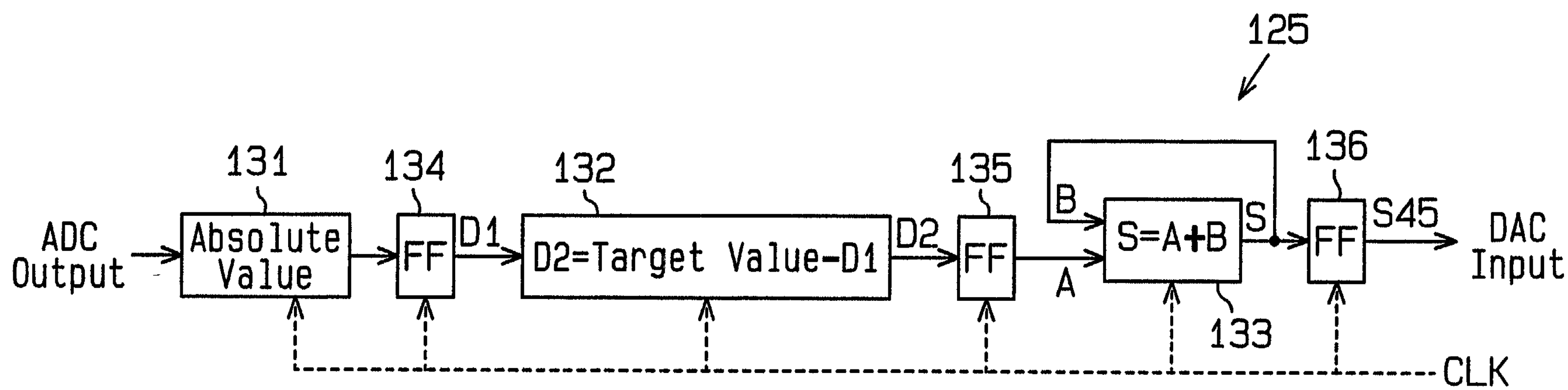


Fig.4(Prior Art)

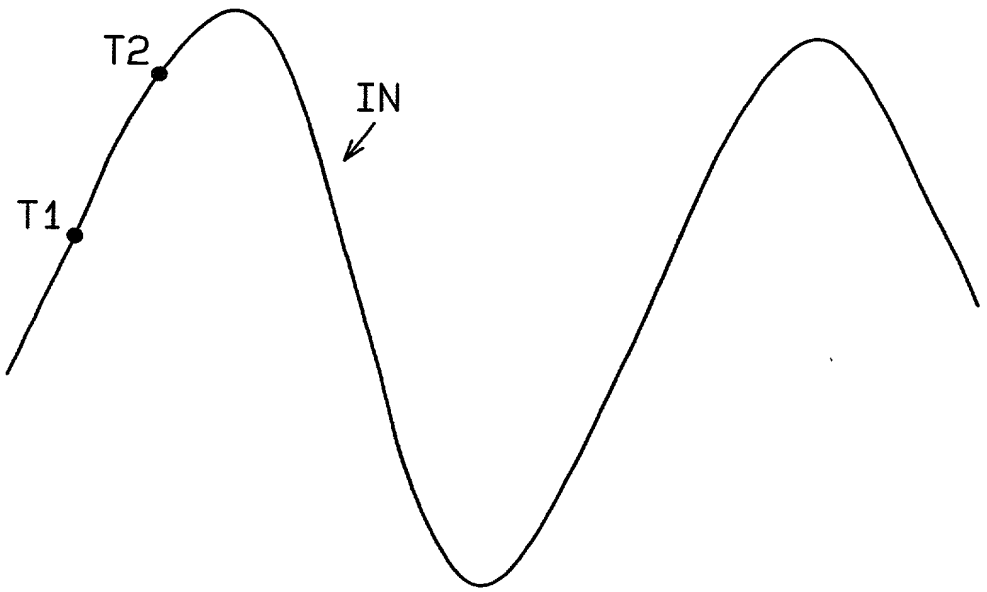


Fig.5

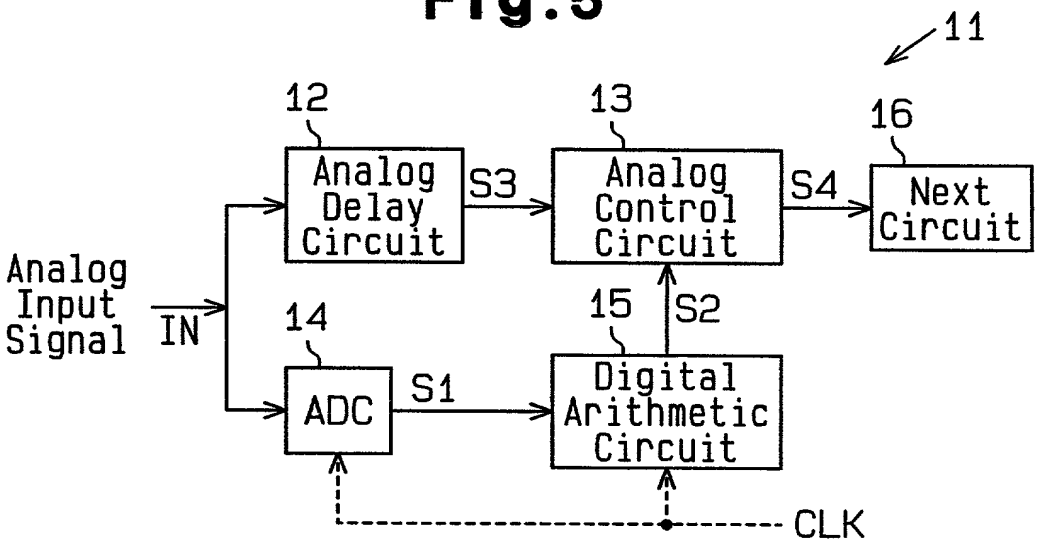

11
12
13
16
Analog Delay Circuit
S3
Analog Control Circuit
S4
Next Circuit
Analog Input Signal
IN
14
15
S2
ADC
S1
Digital Arithmetic Circuit
CLK

Fig.6

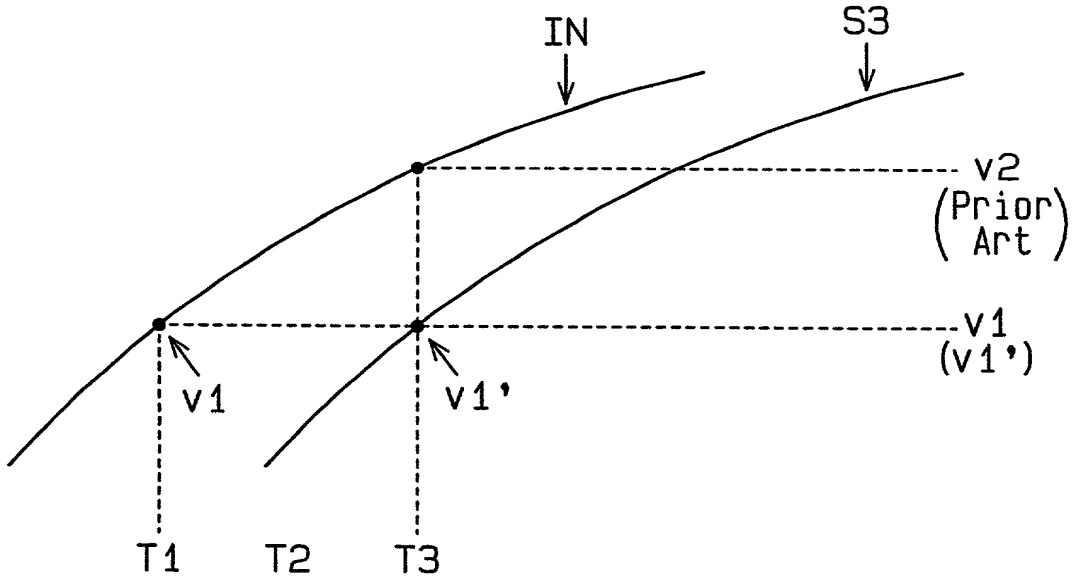

IN
S3
v2
(Prior Art)
v1
(v1')
v1
v1'
T1
T2
T3

Fig.7

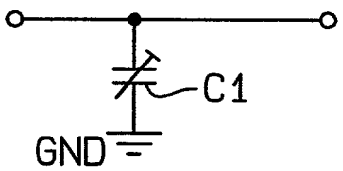


Fig.8

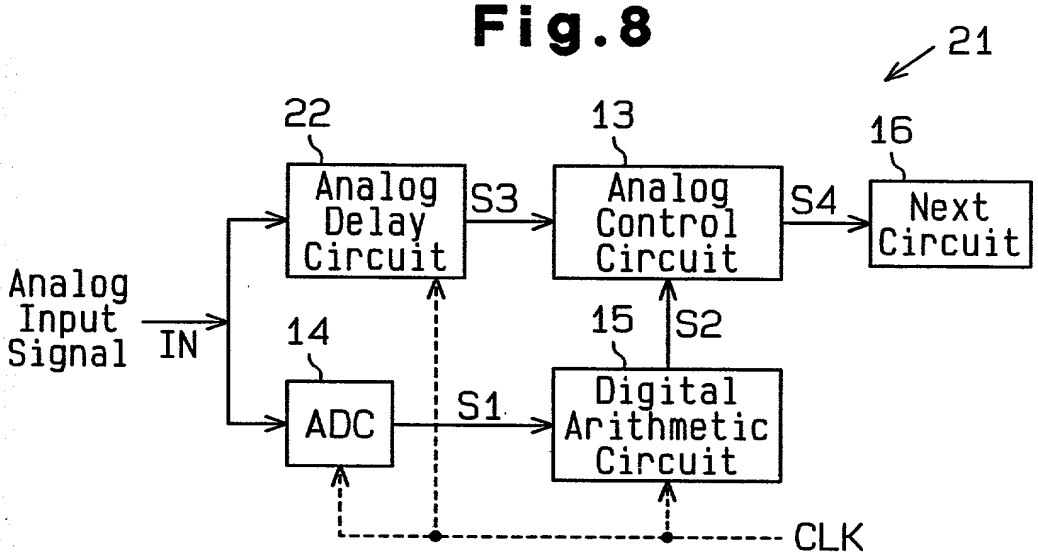


Fig.9

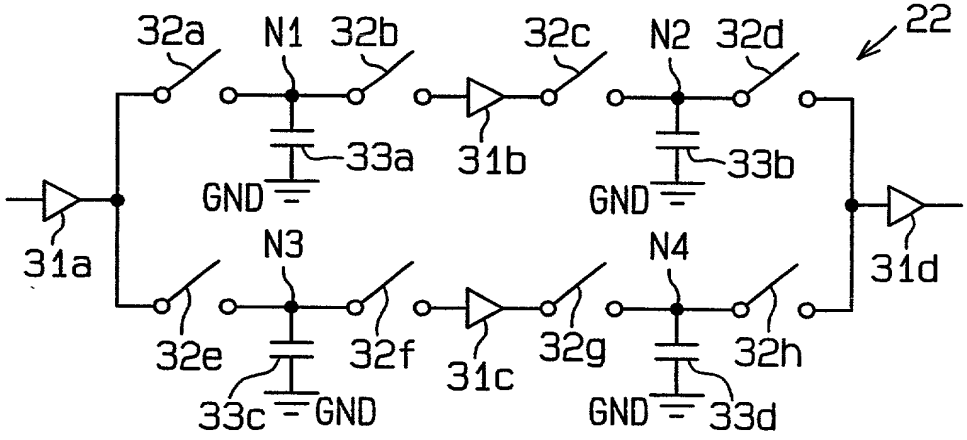


Fig.10

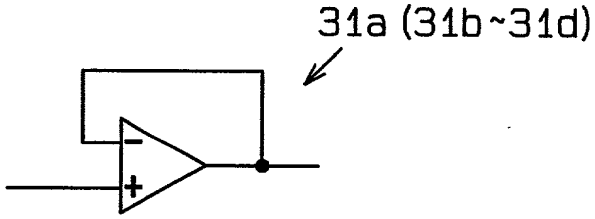


Fig.11

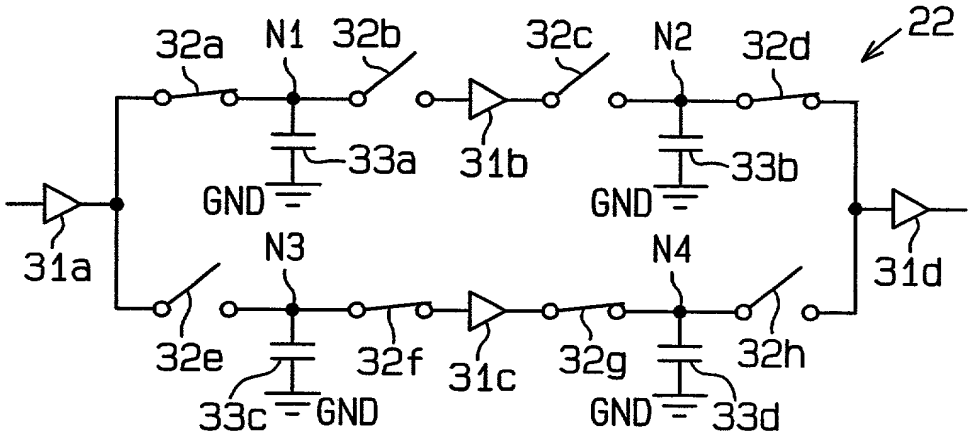


Fig.12

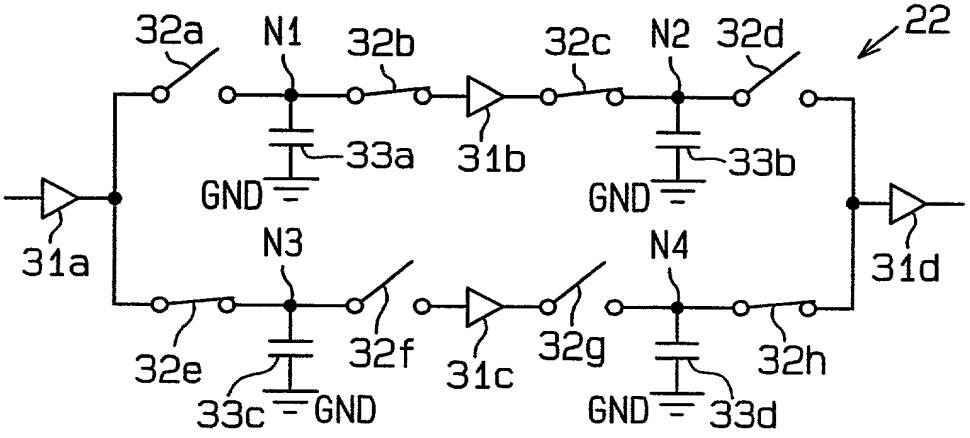
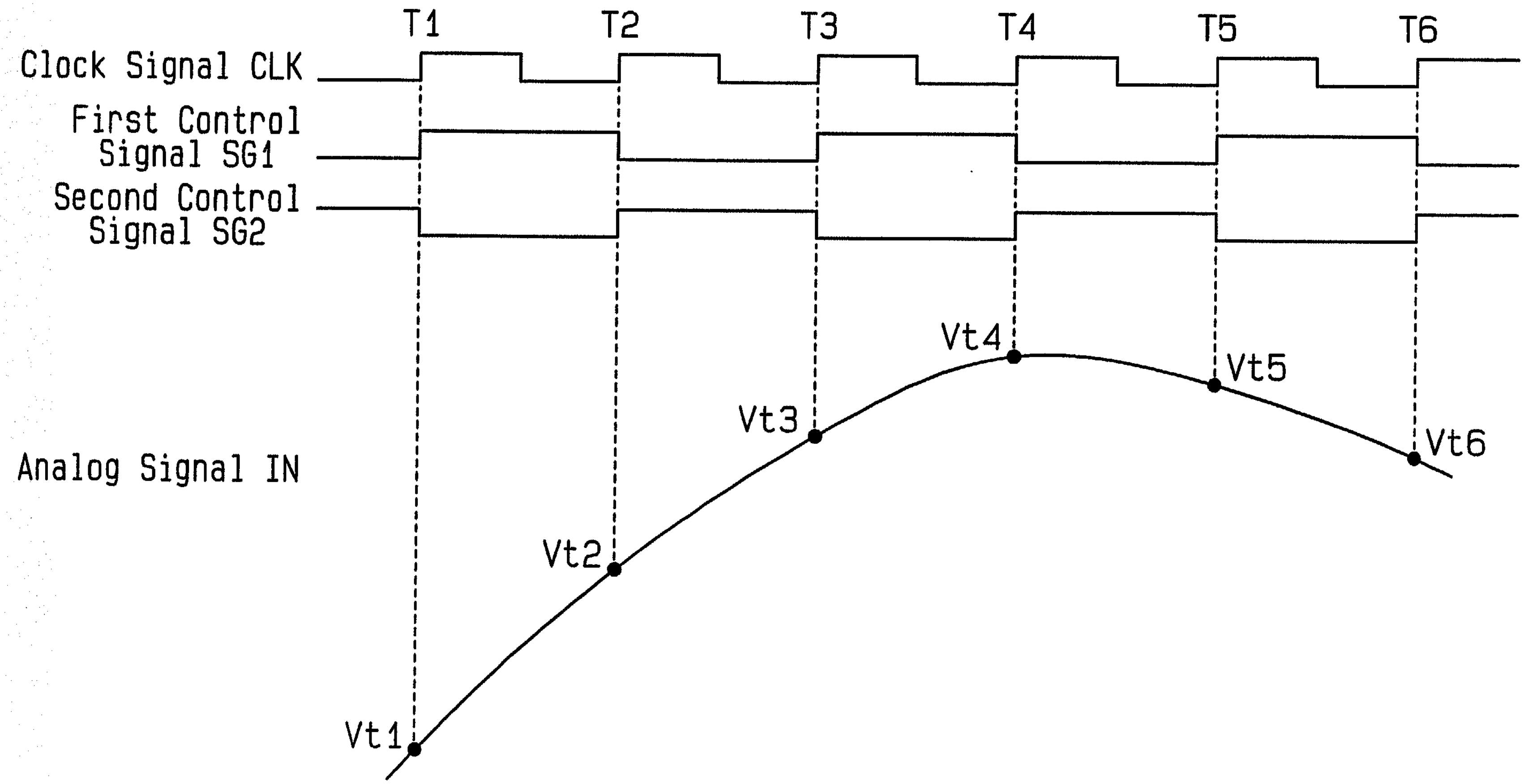


Fig.13



T1
T2
T3
T4
T5
T6
Clock Signal CLK
First Control Signal SG1
Second Control Signal SG2
Analog Signal IN
Vt1
Vt2
Vt3
Vt4
Vt5
Vt6

Fig.14

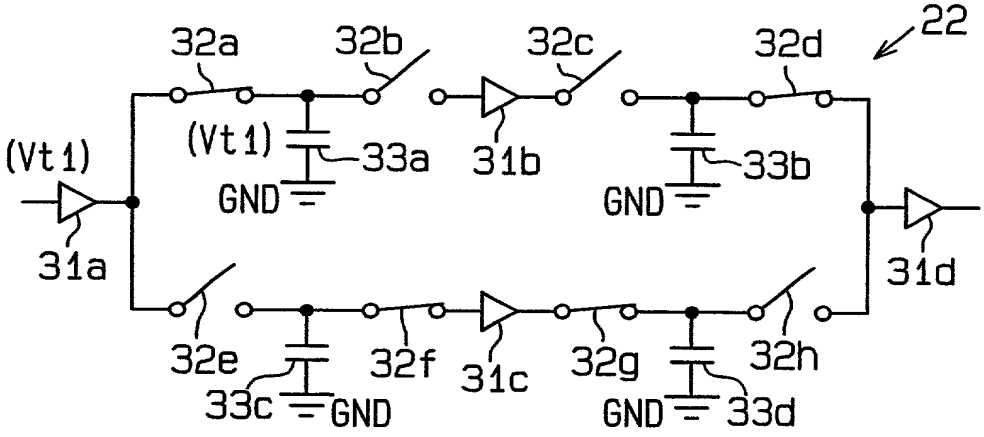


Fig.15

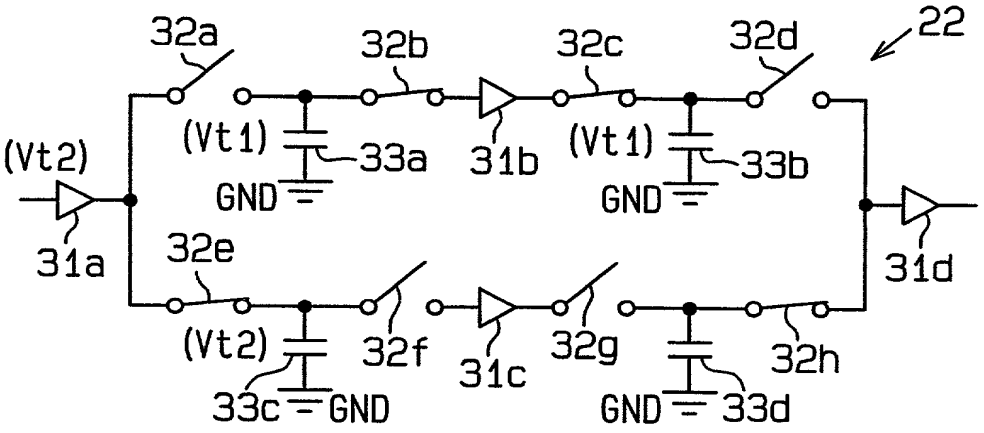


Fig.16

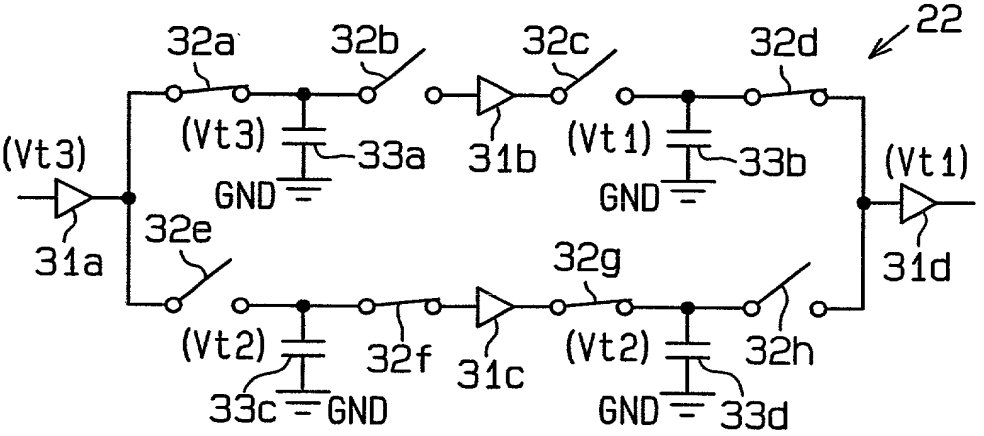


Fig.17

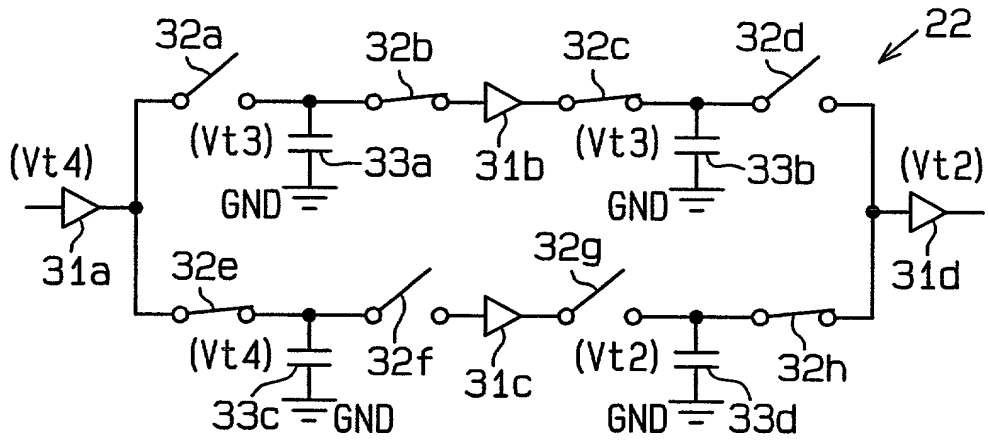


Fig.18

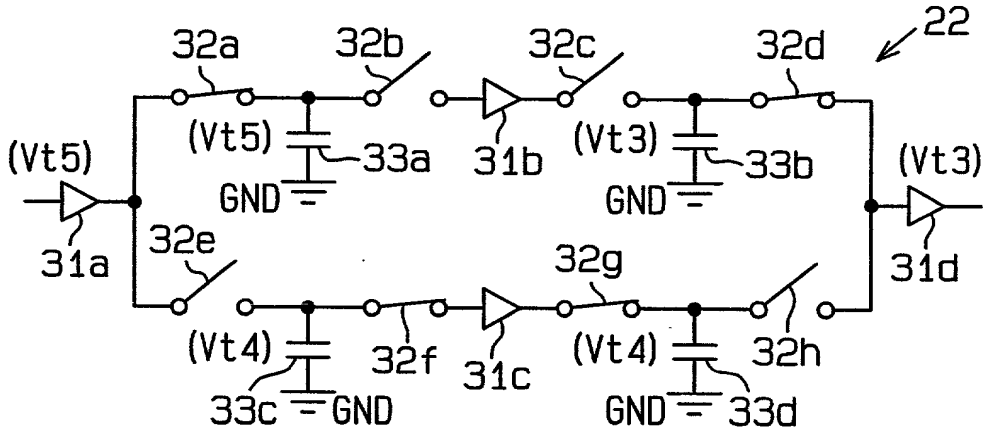


Fig.19

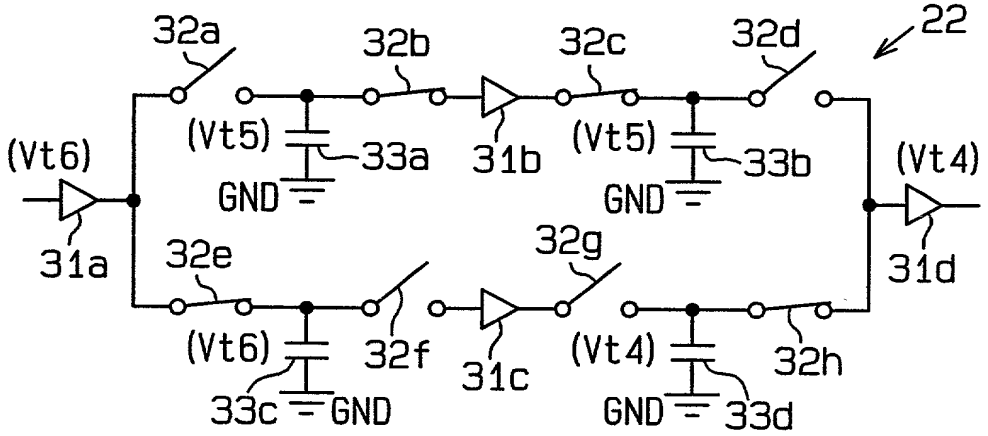


Fig.20

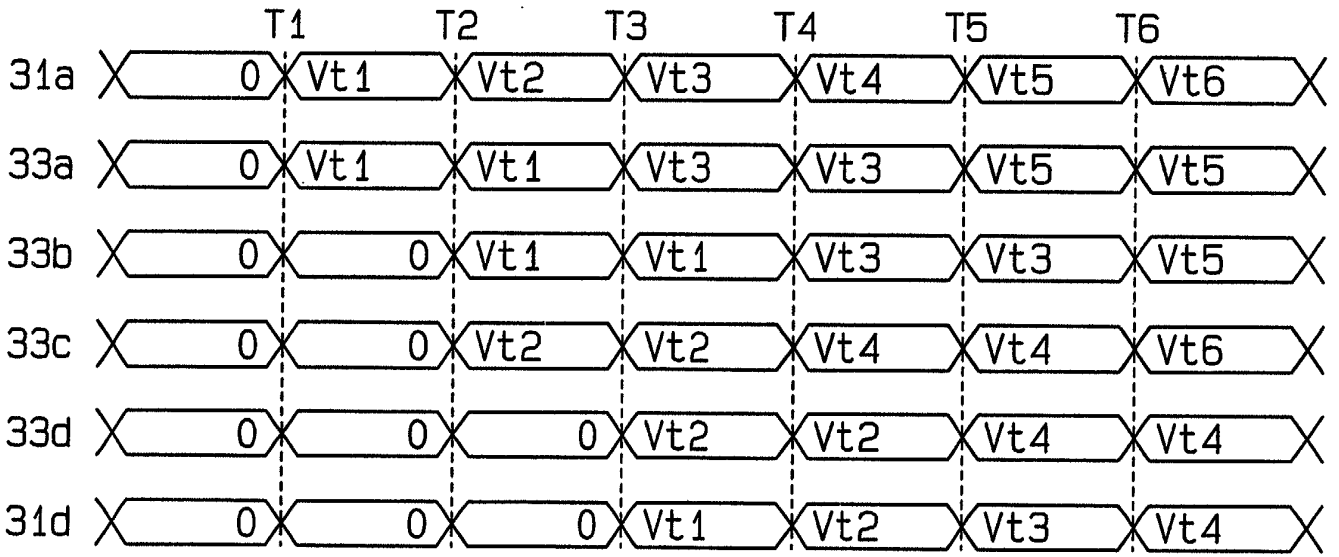

T1
T2
T3
T4
T5
T6
31a
0
Vt1
Vt2
Vt3
Vt4
Vt5
Vt6
33a
0
Vt1
Vt1
Vt3
Vt3
Vt5
Vt5
33b
0
0
Vt1
Vt1
Vt3
Vt3
Vt5
33c
0
0
Vt2
Vt2
Vt4
Vt4
Vt6
33d
0
0
0
Vt2
Vt2
Vt4
Vt4
31d
0
0
0
Vt1
Vt2
Vt3
Vt4

Fig.21

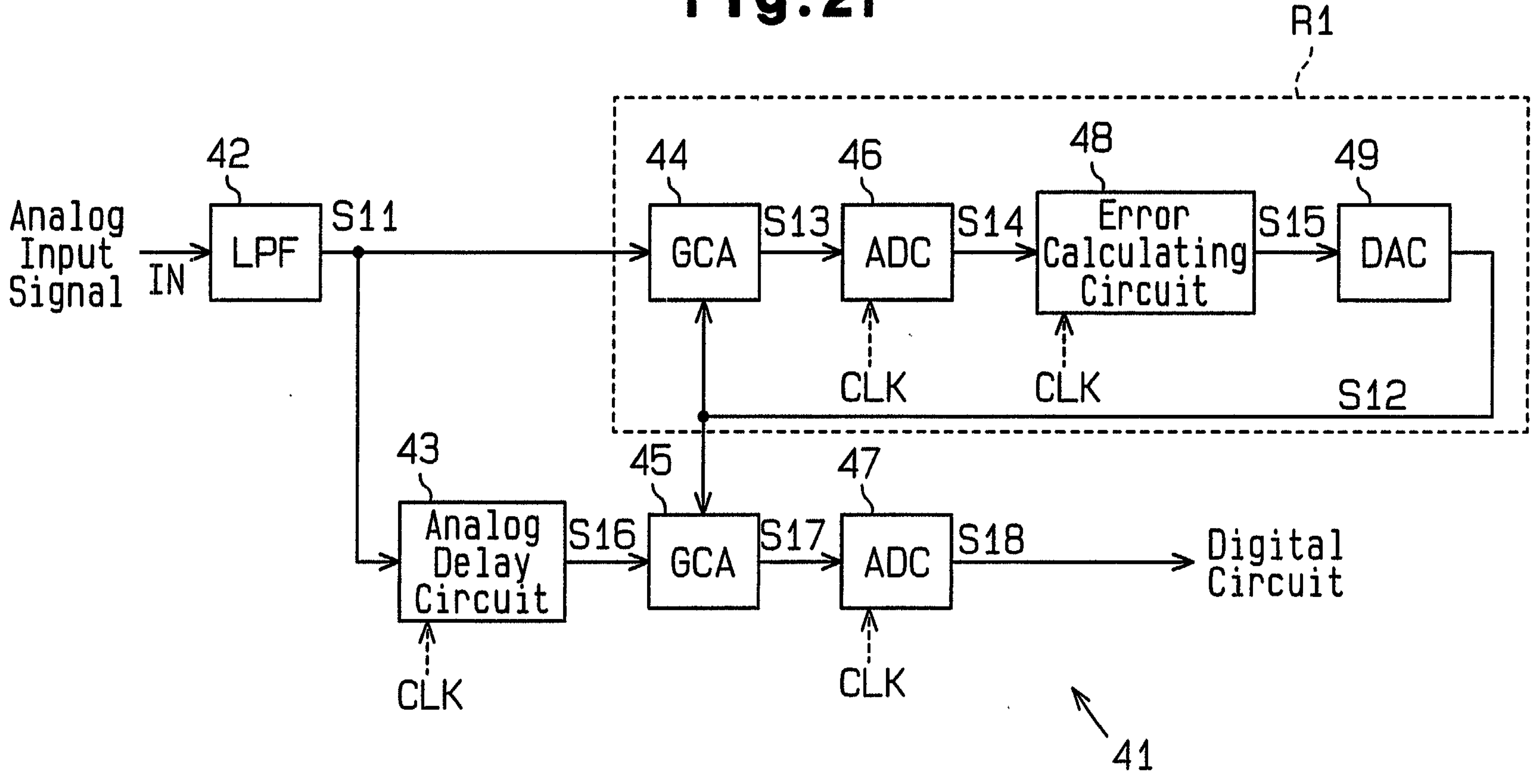
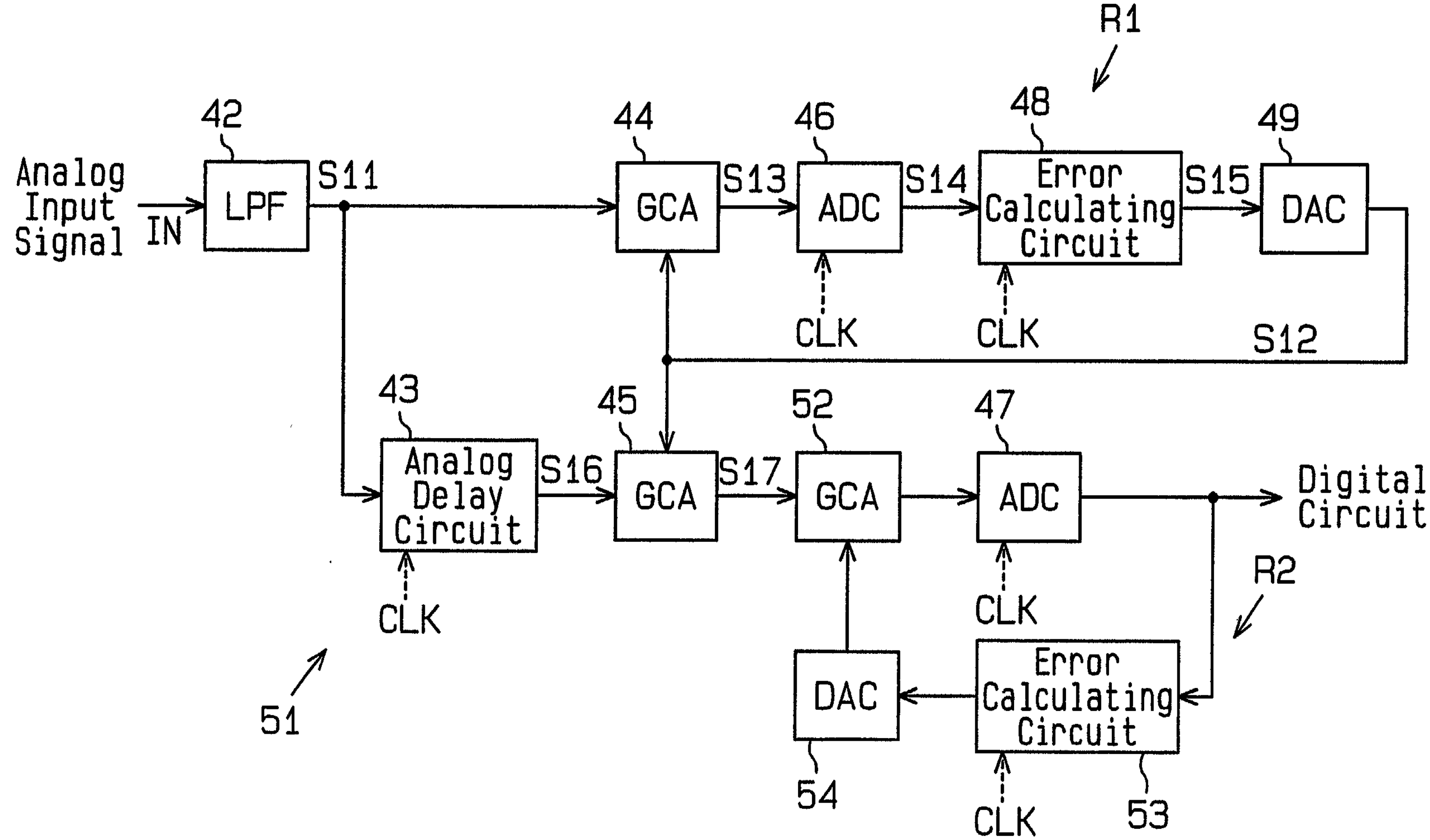

R1
42
44
46
48
49
Analog
Input
Signal
IN
LPF
S11
GCA
S13
ADC
S14
Error
Calculating
Circuit
S15
DAC
CLK
CLK
S12
43
45
47
Analog
Delay
Circuit
S16
GCA
S17
ADC
S18
Digital
Circuit
CLK
CLK
41

Fig.22



Analog Input Signal
IN
42
LPF
S11
44
GCA
S13
46
ADC
S14
48
Error Calculating Circuit
S15
49
DAC
R1
CLK
CLK
S12
43
Analog Delay Circuit
CLK
S16
45
GCA
S17
52
GCA
47
ADC
CLK
Digital Circuit
R2
DAC
54
Error Calculating Circuit
CLK
53
51

Fig.23

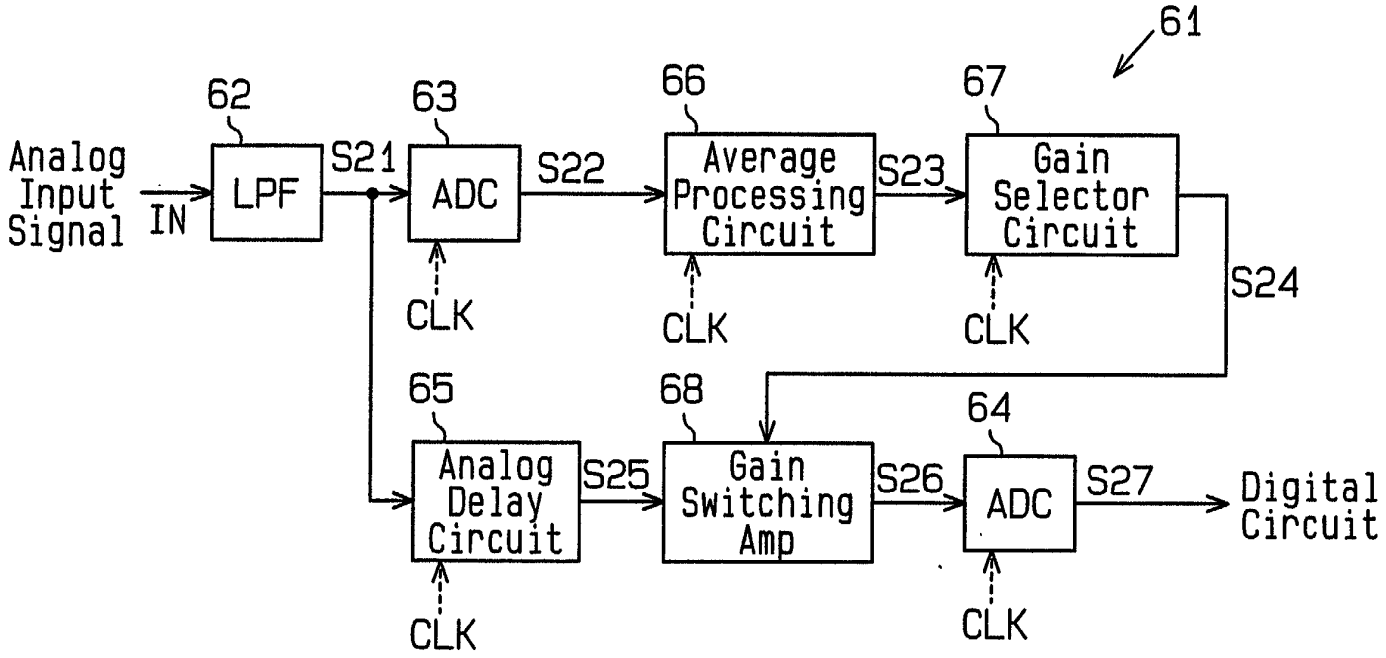

61
62
63
66
67
Analog Input Signal
IN
LPF
S21
ADC
S22
Average Processing Circuit
S23
Gain Selector Circuit
S24
CLK
CLK
CLK
65
68
64
Analog Delay Circuit
S25
Gain Switching Amp
S26
ADC
S27
Digital Circuit
CLK
CLK

Fig.24

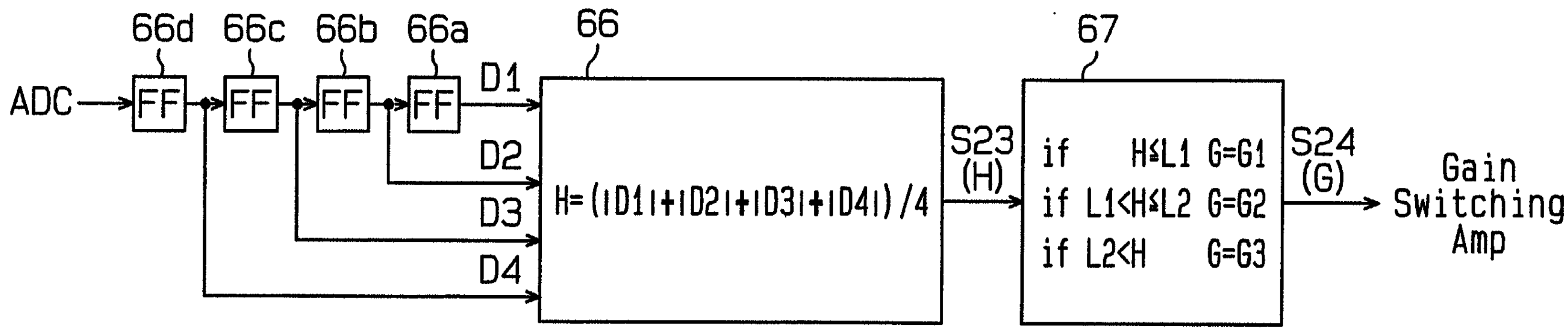

ADC
66d
66c
66b
66a
FF
FF
FF
FF
D1
D2
D3
D4
66
H=(|D1|+|D2|+|D3|+|D4|)/4
S23
(H)
67
if H≤L1 G=G1
if L1<H≤L2 G=G2
if L2<H G=G3
S24
(G)
Gain
Switching
Amp

Fig.25

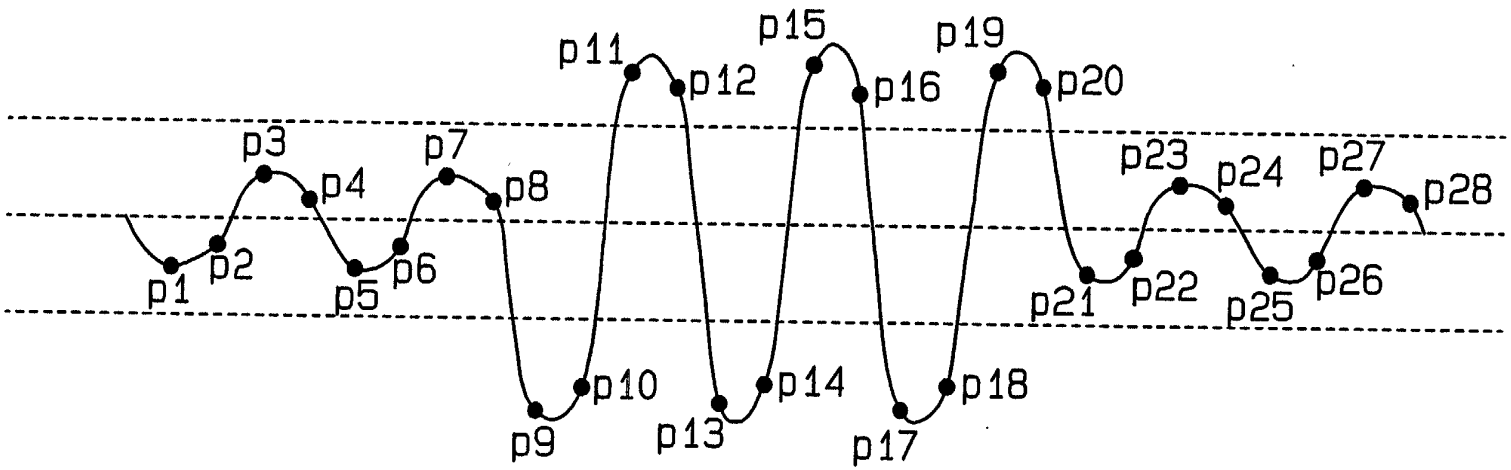
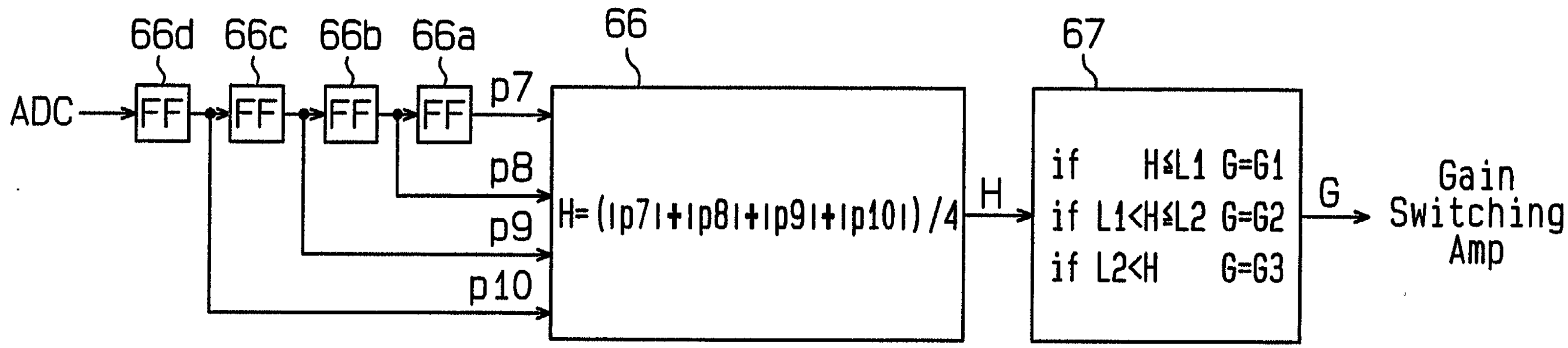
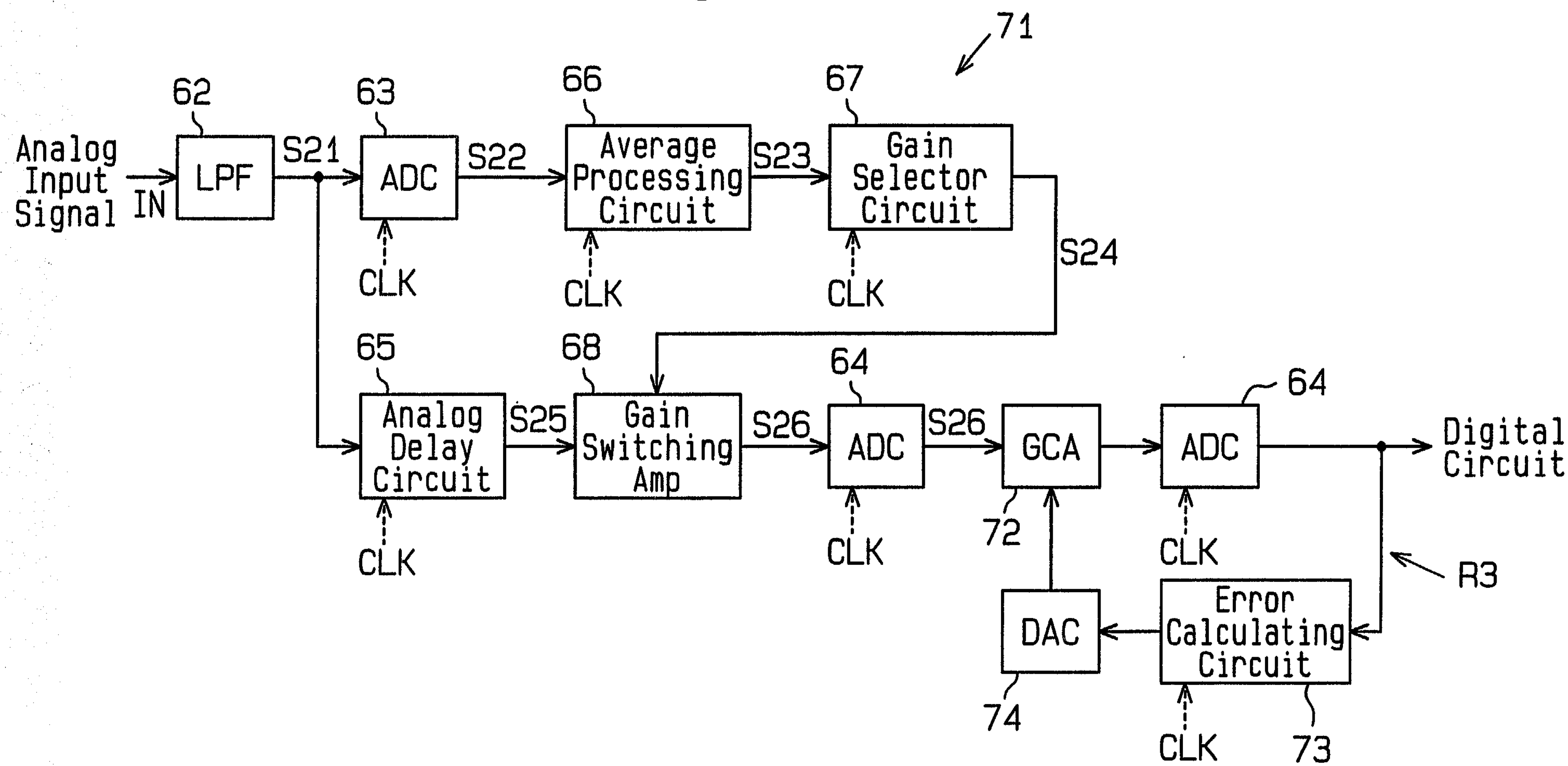


Fig.26



66d
66c
66b
66a
66
67
ADC
FF
FF
FF
FF
p7
p8
p9
p10
H=(|p7|+|p8|+|p9|+|p10|)/4
H
if H≤L1 G=G1
if L1<H≤L2 G=G2
if L2<H G=G3
G
Gain Switching Amp

Fig.27



71
62
63
66
67
Analog
Input
Signal
IN
LPF
S21
ADC
S22
Average
Processing
Circuit
S23
Gain
Selector
Circuit
S24
CLK
CLK
CLK
65
68
64
64
Analog
Delay
Circuit
S25
Gain
Switching
Amp
S26
ADC
S26
GCA
ADC
Digital
Circuit
CLK
CLK
72
CLK
R3
DAC
Error
Calculating
Circuit
74
CLK
73

Fig.28

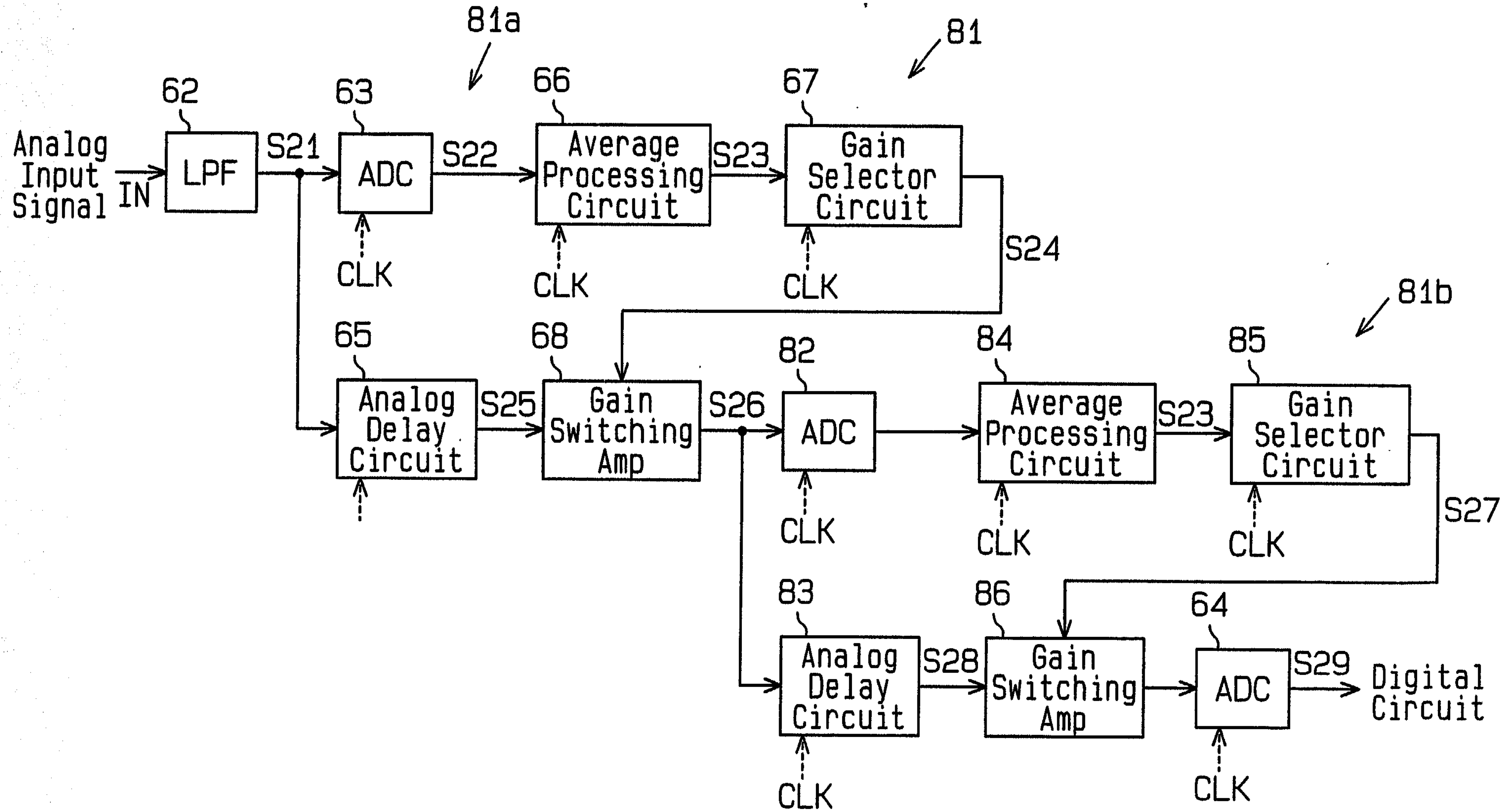
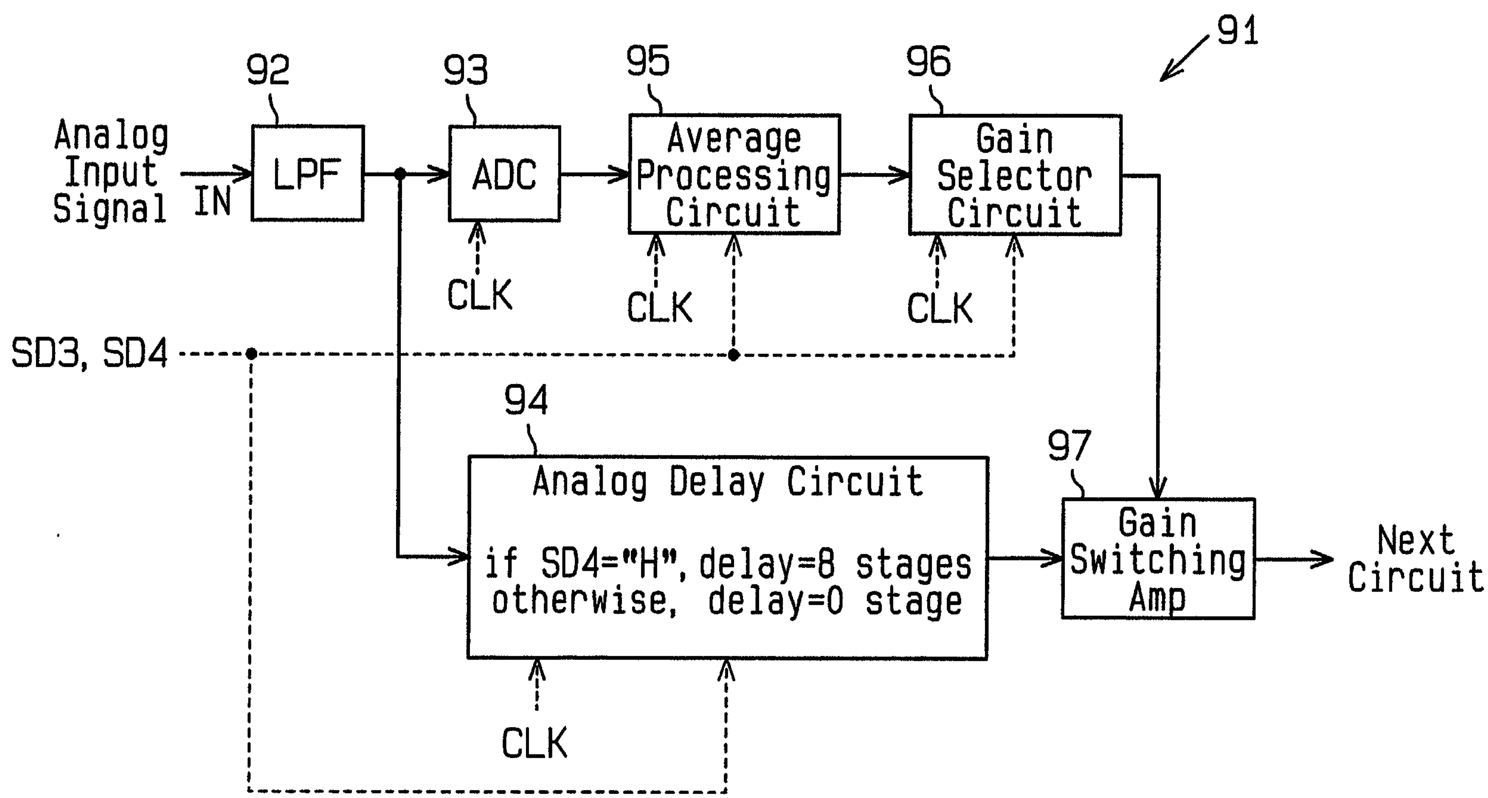

81a
81
81b
62
63
66
67
Analog Input Signal
IN
LPF
S21
ADC
S22
Average Processing Circuit
S23
Gain Selector Circuit
S24
CLK
CLK
CLK
65
68
82
84
85
Analog Delay Circuit
S25
Gain Switching Amp
S26
ADC
Average Processing Circuit
S23
Gain Selector Circuit
S27
CLK
CLK
CLK
83
86
64
Analog Delay Circuit
S28
Gain Switching Amp
ADC
S29
Digital Circuit
CLK
CLK

Fig.29



91
92
93
95
96
Analog Input Signal
IN
LPF
ADC
Average Processing Circuit
Gain Selector Circuit
CLK
CLK
CLK
SD3, SD4
94
97
Analog Delay Circuit
if SD4="H", delay=8 stages
otherwise, delay=0 stage
Gain Switching Amp
Next Circuit
CLK

Fig.30

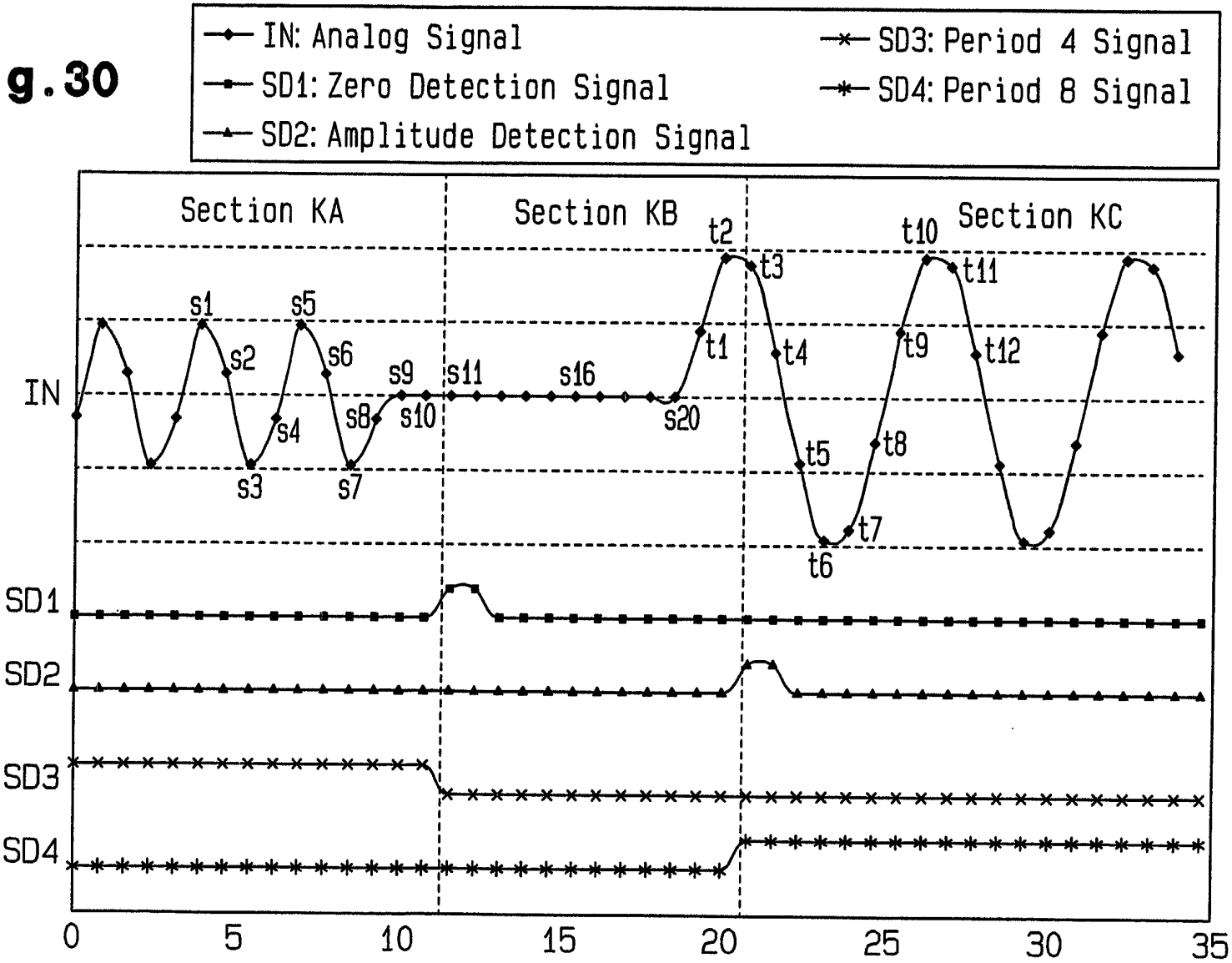
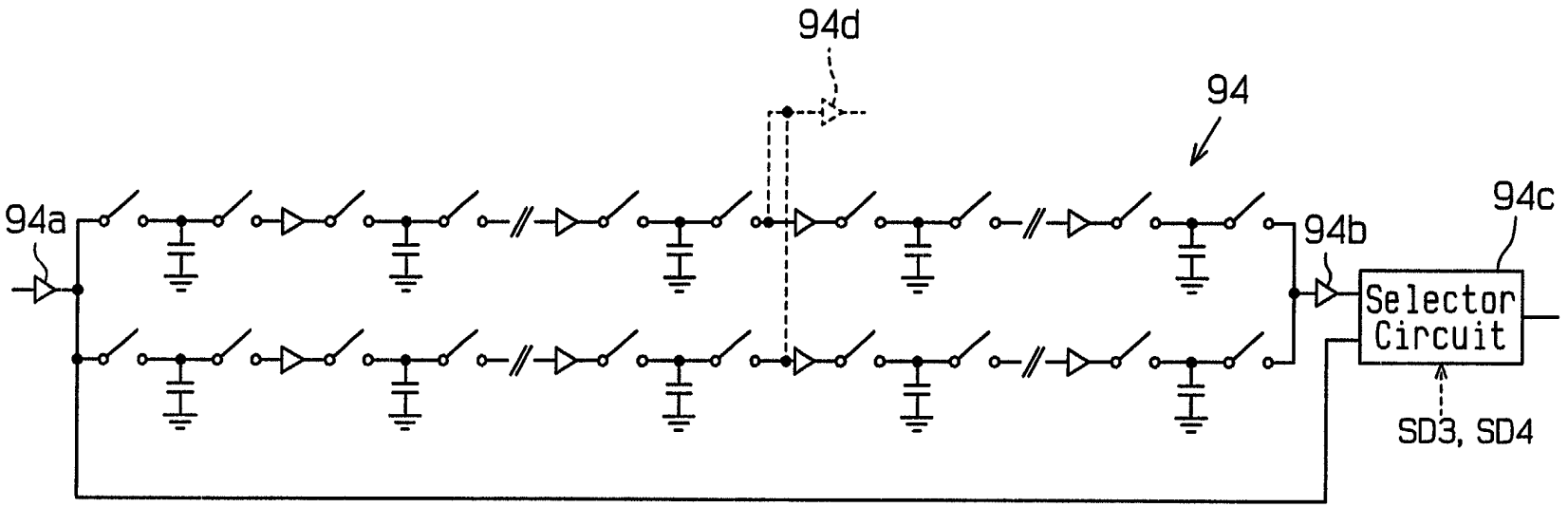

IN: Analog Signal
SD1: Zero Detection Signal
SD2: Amplitude Detection Signal
SD3: Period 4 Signal
SD4: Period 8 Signal
Section KA
Section KB
Section KC
IN
SD1
SD2
SD3
SD4
s1
s2
s3
s4
s5
s6
s7
s8
s9
s10
s11
s16
s20
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
0
5
10
15
20
25
30
35

Fig.31



// Omitted Circuit

Fig.32

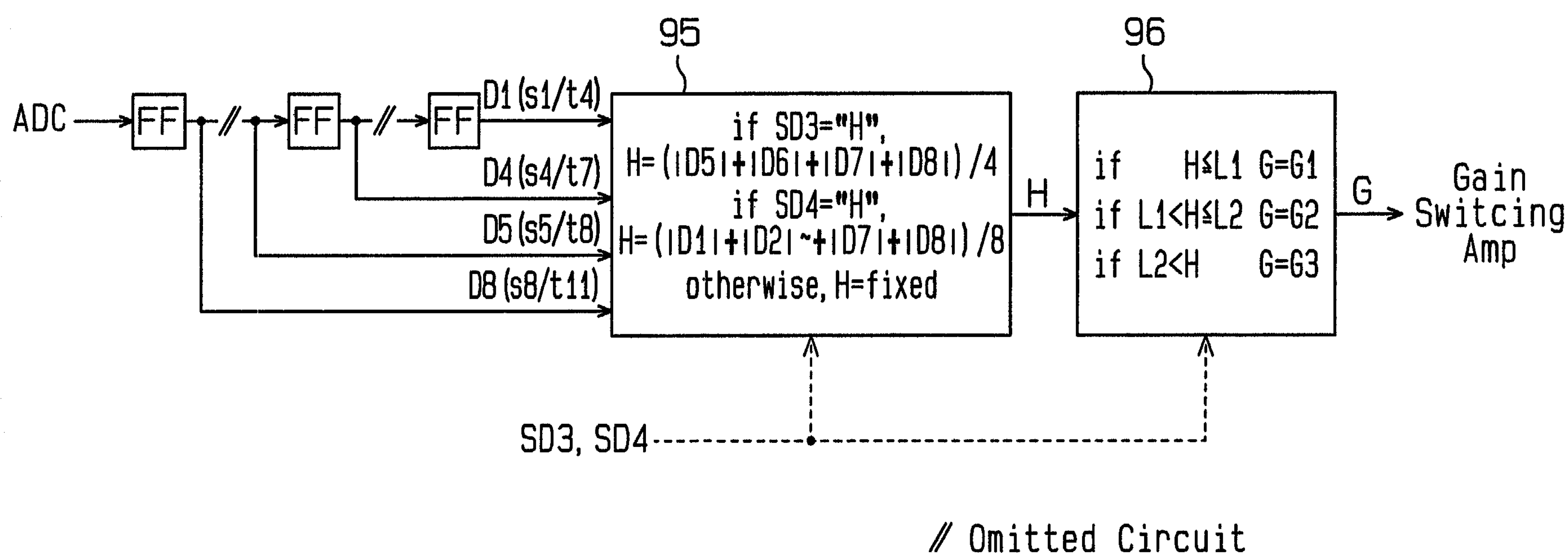
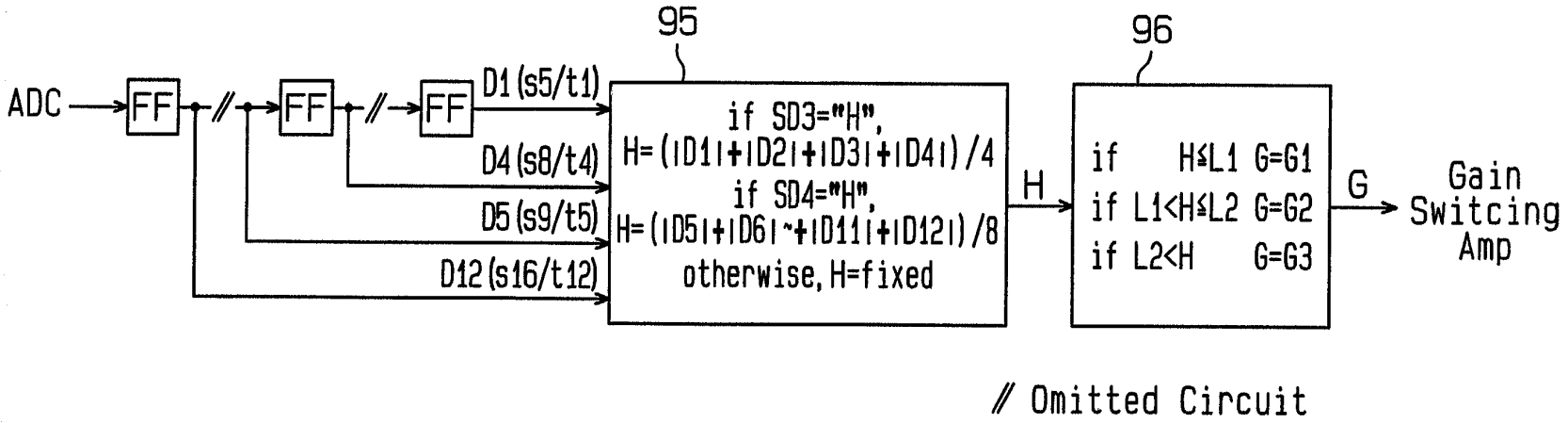

ADC
FF
FF
FF
D1(s1/t4)
D4(s4/t7)
D5(s5/t8)
D8(s8/t11)
95
if SD3="H",
H=(|D5|+|D6|+|D7|+|D8|)/4
if SD4="H",
H=(|D1|+|D2|~+|D7|+|D8|)/8
otherwise, H=fixed
H
96
if H≦L1 G=G1
if L1<H≦L2 G=G2
if L2<H G=G3
G
Gain
Switcing
Amp
SD3, SD4
// Omitted Circuit

Fig.33



// Omitted Circuit

Fig.34

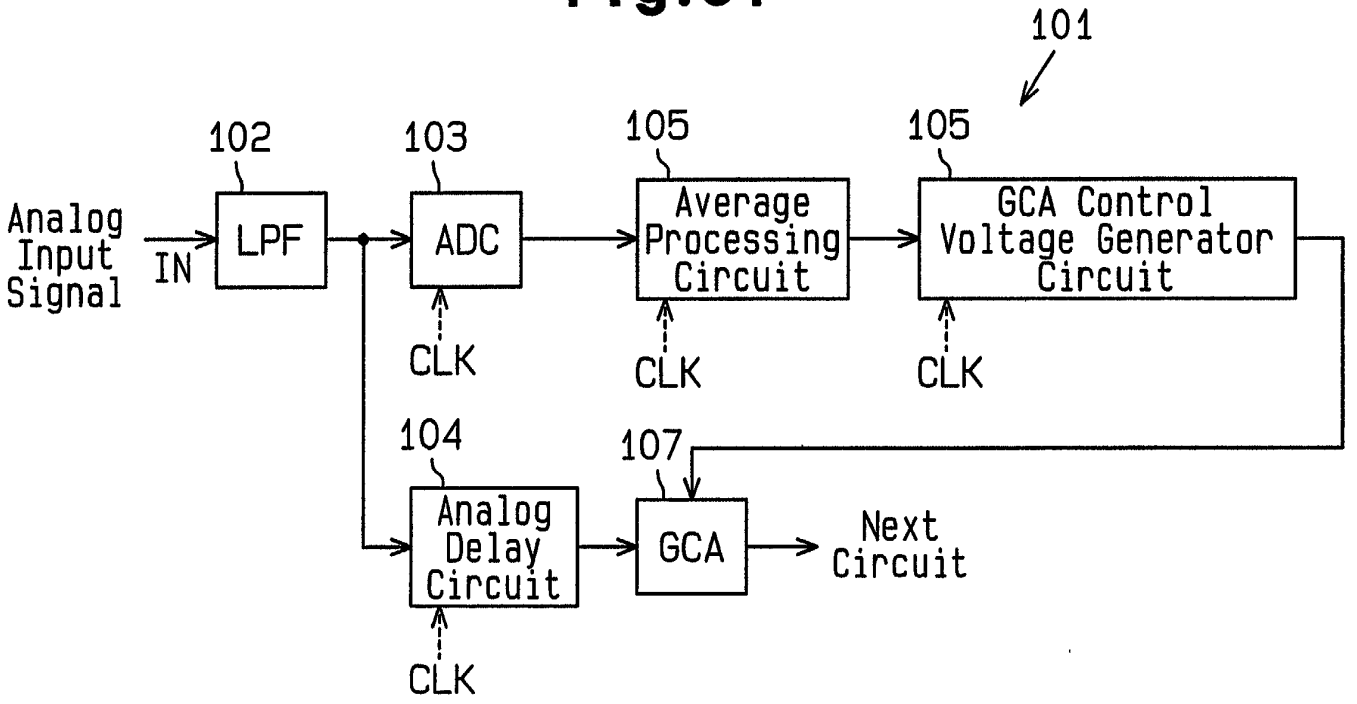

101
102
103
105
105
Analog Input Signal
IN
LPF
ADC
Average Processing Circuit
GCA Control Voltage Generator Circuit
CLK
CLK
CLK
104
107
Analog Delay Circuit
GCA
Next Circuit
CLK

Fig.35